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Search History

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END OF SEARCH HISTORY

Brief Summary Text (86):
It is therefore an object of the present to provide semiconductor test apparatus which conducts a test on a nonvolatile semiconductor storage device such as a flash memory while preventing excessive erasing of data with reliability.

Detailed Description Text (31):
FIG. 5 shows an internal circuit configuration of the error catch memory portion 90. The error catch memory portion 90 of FIG. 5 comprises an address scrambling circuit 110 for translating the logical test address pattern 9 from the address generator 10 into a test pattern corresponding to a physical address of the memory under test 8. This scrambling circuit 110 includes an address-to-be-scrambled selecting circuit 111 (111x for address X, 111y for address Y) for selecting an address signal 112 (112x for address X, 112y for address Y) to be translated into a physical address out of the logical test address pattern 9; a scramble memory circuit 113 (113x for address X, 113y for address Y) for translating the selected address signal 112 into a memory address and storing the translated data; and a scramble address selecting circuit 115 (115x for address X, 115y for address Y) for selecting either a physically converted address signal 114 (114x for address X, 114y for address Y) or the logical address signal 9 in bits of the address. The address scrambling circuit 110 may be provided in the address generator 10.

Detailed Description Text (32):
The address scrambling circuit 110 makes it possible to fetch an error address in testing a memory under test by a physical address pattern for verification of memory cell interference.

Detailed Description Text (62):
The output address signal 181 of the address selecting circuit 179 is synchronized with the synchronizing clock signal 2 in a pipeline circuit 182.alpha.. Then, a selecting circuit 184 selects either an output signal 183 of the pipeline circuit 182.alpha. or the address signal 116 from the address scrambling circuit 110 (cf. FIG. 5) as a test address signal. The selected test address signal is further synchronized with the synchronizing clock signal 2 in a pipeline circuit 182.beta. and outputted as the test address signal 93 of the memory under test 8.

☐ 3. Document ID: US 6191902 B1

L12: Entry 3 of 6 File: USPT Feb 20, 2001

DOCUMENT-IDENTIFIER: US 6191902 B1
**** See image for Certificate of Correction ****
TITLE: Magnetic disk apparatus and magnetic disk medium

Brief Summary Text (5):
In recent years, in association with an increase in capacity of a magnetic disk apparatus as an external storage device of a computer, a magnetic head of a high performance is requested. As a magnetic head satisfying the request, attention is paid to a magnetic disk apparatus having what is called an MR head using a magneto-resistive element which can obtain a high reproduction output without depending on a peripheral velocity of a recording medium. In the magnetic disk apparatus using such an MR head as a read head, however, when the MR head collides with a physical convex or concave portion due to an extremely slight dent, a deformation, or the like on the surface of the medium which is rotating, a temperature of the MR head

rises instantaneously by a friction heat. When the temperature of the MR head rapidly rises by the contact with the medium as mentioned above, a base line of a read signal is shifted, and a read error which cannot be recovered occurs. This state is seemingly the same as when a medium defect exists. The phenomenon in which the read error occurs by the collision heat generation of the MR head with the medium is usually called a thermal asperity. That is, when a state in which a sync byte pattern cannot be read as a result of thermal asperity of the MR head in a sync byte region in a read sector on a medium track, sector data cannot be demodulated at all. In this case, although the reading operation is executed again, since the defect caused by the thermal asperity of the MR head is a kind of physical defects, the same reading impossible state repetitively occurs in the same sync byte region and an unrecoverable read error is caused. For a high density recording of the medium, it is necessary to reduce a floating height of the MR head and this results in a factor of an increase in number of times of occurrence of the defect due to the thermal asperity of the MR head. As a rotational speed of the medium increases, when the thermal asperity of the MR head occurs, the shift of the base line of the read signal further increases. Further, every possible tests have been performed to the magnetic disk apparatus at a factory stage. The defect caused by the thermal asperity of the MR head is, however, a problem occurring during the use by the user. Further, since there is a tendency such that the defect grows while the user is using the apparatus, there is a fear that the performance of the magnetic disk apparatus remarkably deteriorates.

Brief Summary Text (10):
A writing unit (write channel) of a magnetic disk apparatus of the invention splits a sync byte pattern into two patterns of a first sync byte pattern and a second sync byte pattern at the time of writing to a sector region, splits write data into two data of first data and second data, writes the first data subsequently to the first sync byte pattern, writes the second data subsequently to the second sync byte pattern, and finally writes an error detection correction code. When the first sync byte pattern is detected from read data, a reading unit (read channel) demodulates the subsequent first data, second data, and error detection correction code. When the first sync byte pattern is not detected but the second sync byte pattern is detected, the reading unit demodulates the subsequent second data and error detection correction code and reconstructs the lost first data by the error detection correction code. A data length of the first data arranged subsequently to the first sync byte pattern is equal to or longer than a length of defect caused by the thermal asperity of the MR head with the medium and is equal to or shorter than a length of data which can be corrected by the error detection correction code. Even if the loss of data occurs due to the thermal asperity of the MR head, therefore, either one of the split first and second sync byte patterns is lost and sector data can be read out by a normal detection of either one of them. That is, when the first sync byte pattern is lost, the second data and the error detection correction code are normally demodulated by detecting the subsequent second sync byte pattern and the lost first data can be recovered by the error detection correction code without a problem. When the second sync byte pattern is lost, the split data can be read out by detecting the first sync byte pattern without a problem. The first and second sync byte patterns are made different, thereby enabling each pattern to be certainly detected. The writing unit also writes a training pattern for automatically adjusting a circuit constant (tap coefficient) of an automatic equalizer (transversal filter) provided for the reading unit to an optimum value to a position before each of the first and second sync byte patterns. The writing unit also writes a pilot pattern for synchronizing a clock generating circuit provided for the reading unit with the read data to a position before each of the first and second sync byte patterns. Further, the writing unit has a scrambling circuit for scrambling each of the first and second data and, further, the error detection correction code to be written to the medium by using a predetermined pseudo random code (for example, M series code). In correspondence to the scrambling circuit, the reading unit has a descrambling circuit for descrambling the first and second data and the error detection correction code read

out from the medium by using the pseudo random code. A gap pattern at a sector boundary can be also scrambled and descrambled.

Brief Summary Text (15):
The writing unit has a scrambling circuit for scrambling each of the first to fourth data and the error detection correction code which are written to the medium by using a predetermined pseudo random code. Simultaneously, the reading unit has a descrambling circuit for descrambling each of the first to fourth data and the error detection correction code read out from the medium by using the pseudo random code. In case of the data split, when the first sync byte pattern is detected with respect to the first sector region, after the first data was demodulated, the reading unit skips the demodulation of the second sync byte pattern and demodulates the second data. Subsequently, when the first sync byte pattern is detected with respect to the second sector region, after demodulating the third data, the demodulation of the second sync byte pattern is skipped, and the fourth data and the error detection correction code are demodulated. Specifically speaking, the reading unit presets a data length of the first or third data, a gap length from the first data to the second data, and a gap length from the third data to the fourth data. With respect to the first sector region, the first data is demodulated for an interval of the data length from the end of the detection of the first sync byte pattern, skips the pattern detection for an interval of the gap length, and after that, starts the demodulation of the second data. Subsequently, with respect to the second sector region, the third data is demodulated for an interval of the data length from the end of the detection of the first sync byte pattern, the pattern detection is skipped for an interval of the gap length, and after that, the demodulation of the fourth data is started. With respect to the data split, when the first sync byte pattern in the first sector region is not detected but the second sync byte pattern is detected, the reading unit demodulates the subsequent second to fourth data and the error detection correction code and reconstructs the first data by the error detection correction code. As for the data split, in the case where the first and second data in the first sector region are normally demodulated and the first sync byte pattern is not detected upon reading of the second sector region and the third data is lost and the second sync byte pattern is detected, the reading unit demodulates the subsequent fourth data and the error detection correction code and reconstructs the third data by the error detection correction code. Further, with regard to the data split, when both of the first and second sync byte patterns in the first sector region or both of the first and second sync byte patterns in the second sector region cannot be detected, the reading unit performs the rereading process. In the case where the first sector region cannot be demodulated and the process is shifted to the rereading process, rereading process, the reading unit turns on the read gate by the detection of the first pilot pattern subsequent to the first data and starts the pattern detection. When the second sync byte pattern is detected, the reading unit demodulates the subsequent second to fourth data and the error detection correction code and reconstructs the first data by the error detection correction code. In the case where the second sector region cannot be demodulated and the process is shifted to the rereading process, after the first and second data in the first sector region are demodulated, the reading unit turns on the read gate by the detection of the pilot pattern subsequent to the third data and starts the pattern detection. When the second sync byte pattern is detected, the reading unit demodulates the subsequent fourth data and the error detection correction code and reconstructs the third data by the error detection correction code.

Detailed Description Text (34):
FIG. 21 shows another embodiment of the write channel 19 in FIG. 1. The embodiment is characterized in that data, ECC, and gap pattern to be written to the disk medium are scrambled. In a manner similar to the embodiment of FIG. 2A, the write channel 19 is made up of the HDC interface circuit 60 for writing, 8/9 encoder 62, parallel/serial converter 64, precoder 66, frequency divider 68, and driver 70. A circuit function to scramble the data, ECC, and gap pattern is provided between the

HDC interface circuit 60 for writing and the 8/9 encoder 62. That is, a scrambling circuit 172 is provided after the HDC interface circuit 60 for writing. The scrambling circuit 172 has an EX-OR circuit 174 and a pseudo random pattern generator 176. The pseudo random pattern generator 176 generates, for example, an M series code of a predetermined code length. The EX-OR circuit 174 gets the EX-OR between the formatted data of one sector from the HDC interface circuit 60 for writing and the pseudo random pattern, thereby scrambling. A selecting circuit 170 is provided after the scrambling circuit 172. The data from the HDC interface circuit 60 for writing and the data scrambled by the scrambling circuit 172 are inputted to the selecting circuit 170. Either one of these is selected and inputted to the 8/9 encoder 62. The selecting circuit 170 selects the data scrambled by the scrambling circuit 172 at a timing of the write data ECC and gap pattern. At the other timings, the selecting circuit 170 selects the data from the HDC interface circuit 60 for writing, namely, the data which is not scrambled. The selecting operation of the selecting circuit 170 and the generation of the pattern of the pseudo random pattern generator 176 are controlled by a timing generating circuit 184. A sync byte detecting circuit 178, a DL register 180, and a GL register 182 are provided for the timing generating circuit 184. The sync byte detecting circuit 178 detects the first and second sync byte patterns SB1 and SB2 included in the formatted write data derived from the HDC interface circuit 60 for writing and outputs them. The data length DL of the first data DATA1 subsequent to the first sync byte pattern SB1 has been set in the DL register 180. An interval of the first data DATA1 according to the data length DL set in the DL register 180 is set from the timing when the sync byte detecting circuit 178 detects the first sync byte pattern SB1. The gap data length GL from the end of the first data DATA1 to the beginning of the next second data DATA2 has been set in the GL register 182. In response to those lengths, the timing generating circuit 184 sets a scrambling period of time for an interval of the second data DATA2, ECC, and next gap pattern. Timing signals indicative of the timings of the first data, second data, ECC, and gap pattern to be scrambled which are generated from the timing generating circuit 184 are also given to the pseudo random pattern generator 176. A pseudo random pattern is generated from the pseudo random pattern generator 176 to the EX-OR circuit 174 synchronously with an output selection from the scrambling circuit 172 of the selecting circuit 170, thereby enabling the scrambled data to be supplied to the selecting circuit 170.

Detailed Description Text (35):
FIGS. 22A to 22E are time charts for the scrambling process of the write channel 19 in FIG. 21. First, when the write gate signal 81 in FIG. 22A is turned on, the pseudo random pattern generator 176 of the scrambling circuit 172 is made operative. In this state, the write data according to the HDC data format as shown in FIG. 22B is inputted to the write channel 19 through the HDC interface circuit 60 for writing.

Detailed Description Text (36):
The first sync byte detecting circuit 178 detects the sync byte pattern 88 shown at SB1 and outputs a detection signal to the timing generating circuit 184. In response to it, the timing generating circuit 184 generates the timing signal to the selecting circuit 170 for an interval of the data length DL set in the DL register 180, thereby allowing the output of the scrambling circuit 172 to be selected. Since the timing signal is supplied to the pseudo random pattern generator 176, a scramble signal 188-1 in FIG. 22D is generated, so that the first data 90 shown by DATA1 is scrambled by the EX-OR circuit 174. Subsequently, the generation of the timing signal from the timing generating circuit 184 is stopped for the setting interval of the gap length GL by the GL register 182 and the pseudo random pattern generator 176 is reset. After the elapse of the gap length GL, the timing signal generating circuit 184 again generates a timing signal 186-2 as shown in FIG. 22C for an interval from the head of the second data 98 shown by DATA2 to the end of the gap data 101 after the ECC 100. Therefore, as shown in FIG. 22D, a scramble signal 188-2 is generated on the basis of the timing signal 186-2, thereby

scrambling.

Detailed Description Text (38):
FIG. 23 is a block diagram of the embodiment having a descrambling function of the read channel 20 in FIG. 1 corresponding to the write channel 19 having the scrambling function of FIG. 21. The read channel 20 has the amplifier 72, AGC circuit 74, automatic equalizing type maximum likelihood detecting circuit 76, 8/9 decoder 78, serial/parallel converter 79, and HDC interface circuit 80 for reading in FIG. 2B. Further, a descrambling circuit 190 and a selecting circuit 204 are provided between the serial/parallel converter 79 and the HDC interface circuit 80 for reading. An EX-OR circuit 192 and a pseudo random pattern generator 194 are provided for the descrambling circuit 190 and are substantially the same as the scrambling circuit 172 in FIG. 22. The selecting operation of the selecting circuit 204 is controlled by a timing generating circuit 205. That is, the selecting circuit 204 selects an output of the descrambling circuit 190 at the timing of the first data DATA1, second data DATA2, ECC, and gap pattern included in the read data, thereby descrambling. At the other timings, the selecting circuit 204 directly selects the output of the serial/parallel converter 79, thereby cancelling the descrambling state. A first sync byte detecting circuit 196 and a second sync byte detecting circuit 198 are provided for controlling the serial/parallel converter 79, pseudo random pattern generator 194, and timing control generating circuit 205. Further, a DL register 200 in which the data length DL of the first data DATA1 has been stored and a GL register 202 in which the gap length GL from the first data DATA1 to the second data DATA2 has been stored are provided in order to control the timing generating circuit 205.

CLAIMS:

1. A magnetic disk apparatus for writing and reading information onto/from tracks of a medium on a sector unit basis by using a combination head having a write head and a read head, comprising:

a writing unit for forming format data including first data having a data length DL which can be corrected by an error detection correction code, a first sync byte pattern arranged just before said first data second data arranged at a predetermined gap length GL from said first data, second sync byte data arranged just before said second data, and said error detection correction code arranged subsequently to said second data, and for writing said format data onto said medium with the write head at the time of writing into a sector region;

a scrambling circuit, provided for said writing unit, for turning on a scrambling operation by a detection of said first sync byte pattern of said write format data, subsequently turning off said scrambling operation at an elapsed timing of said data length DL, again turning on said scrambling operation at a next elapsed timing of said gap length GL, subsequently turning off said scrambling operation at a sector end timing after said error detection correction code, and scrambling each of said first data, said second data, and said error detection correction code in said write format data;

a reading unit for reading out said format data including said first data having said data length DL, said first sync byte pattern arranged just before said first data, said second date arranged at said predetermined gap length GL from said first data, said second sync byte data arranged just before said second data, and said error detection correction code arranged subsequently to said second data at the time of reading out from said sector region; and subsequently demodulating said first data and said second data in the case where said first sync byte pattern is detected, and subsequently demodulating said second data and said error detection correction code in the case where said first sync byte pattern is not detected but said second sync byte pattern is detected and reconstructing said first data using said error detection correction code; and

a descrambling circuit provided for said reading unit and constructed in such a manner that in the case where said first sync byte pattern of said format data is detected, a descrambling operation is turned on at the time of said detection and turned off at the elapsed timing of said data length DL, said descrambling operation being subsequently again turned on at the elapsed timing of said gap length GL and turned off at the sector end timing after said error detection correction code, thereby descrambling each of said first data, said second data, and said error detection correction code which are included in said write format data, and in the case where said first sync byte pattern of said format data is not detected but said second sync byte pattern is detected, said descrambling operation is turned on at the time of said detection and turned off at the sector end timing after said error detection correction code, thereby descrambling each of said second data and said error detection correction code which are included in said write format data.

14. A magnetic disk medium adapted to be provided in a magnetic disk apparatus including a scrambling circuit and a descrambling circuit and being subjected to operations for writing and reading information onto/from tracks on a sector unit basis by using a combination head having a write head and a read head, said disk medium comprising:

format data including first data having a data length DL which can be corrected by an error detection correction code, a first sync byte pattern arranged just before said first data second data arranged at a predetermined gap length GL from said first data, second sync byte data arranged just before said second data, and said error detection correction code arranged subsequently to said second data;

wherein said first data, said second data, and said error detection correction code are written scrambled onto said disk medium by the scrambling circuit which turns on a scrambling operation by a detection of said first sync byte pattern of said format data, subsequently turns off the scrambling operation at an elapsed timing of said data length DL, again turns on the scrambling operation at a next elapsed timing of said gap length GL, and subsequently turns off the scrambling operation at a sector end timing after said error detection correction code, and said first data and said second data are adapted to be demodulated when said first sync byte pattern is detected at the time said sector region is read, and said second data is adapted to be demodulated when said first sync byte pattern is not detected but said second sync byte pattern is detected, so that said first data can be reconstructed using said error detection correction code.

☐ 4. Document ID: US 6147826 A

L12: Entry 4 of 6 File: USPT Nov 14, 2000

DOCUMENT-IDENTIFIER: US 6147826 A
TITLE: Magnetic disk apparatus having duplicate sync byte patterns

Brief Summary Text (3):
In recent years, in association with an increase in capacity of a magnetic disk apparatus as an external storage device of a computer, a magnetic head of a high

performance is needed. As a magnetic head satisfying the need, attention is paid to a magnetic disk apparatus having what is called an MR head using a magneto-resistive element which can obtain a high reproduction output without depending on a peripheral velocity of a recording medium. In the magnetic disk apparatus using such an MR head as a read head, however, when the MR head collides with a physical convex or concave portion due to an extremely slight dent, a deformation, or the like on the surface of the medium which is rotating, a temperature of the MR head rises instantaneously by a friction heat. When the temperature of the MR head rapidly rises by the contact with the thermal fluctuation concave and convex portions of the medium as mentioned above, a base line of a read signal is shifted, and a read error which cannot be recovered occurs. This state is seemingly the same as that a medium defect exists. The phenomenon in which the read error occurs by the collision heat generation of the MR head with the medium is usually called a thermal asperity. That is, when a state in which a sync byte pattern cannot be read by the thermal asperity of the MR head occurs in a sync byte region in a read sector on a medium track, sector data cannot be demodulated at all. In this case, although the reading operation is executed again, since the thermal fluctuation concave and convex portions are kind of physical defects, the same reading impossible state repetitively occurs in the same sync byte region and an unrecoverable read error is caused. For a high density recording of the medium, it is necessary to reduce a floating height of the MR head and this results in a factor of an increase in number of times of occurrence of the defect due to the thermal asperity of the MR head. As a rotational speed of the medium increases, when the thermal asperity of the MR head occurs, the shift of the base line of the read signal further increases. Further, every possible is performed on the magnetic disk apparatus at the factory. The defect caused by the thermal asperity of the MR head is, however, a problem occurring during the use by the user. Further, since there is a tendency such that the defect grows while the user is using the apparatus, there is a fear that the performance of the magnetic disk apparatus remarkably deteriorates.

Brief Summary Text (11):
The writing unit writes a training pattern for automatically adjusting circuit constants (tap coefficients and the like of a transversal filter) of an automatic equalizer provided for the reading unit to optimum values to a position before each of the first and second sync byte patterns SB1 and SB2. The writing unit writes a pilot pattern for synchronizing a clock generating circuit provided for the reading unit with a read signal to a position before the first sync byte pattern SB1. Further, the writing unit has a scrambling circuit for scrambling each of the data and ECC (error detection correction code) which are written to the medium by using a predetermined pseudo random code. It is necessary to turn off the scrambling operation for the second sync byte pattern SB2 and gap pattern. In correspondence to it, the reading unit has a descrambling circuit for descrambling each of the data and ECC read out from the medium by using the pseudo random code. The reading unit executes the reading process again when both of the first and second sync byte patterns SB1 and SB2 cannot be detected. When the first sync byte pattern SB1 cannot be detected, after the reading process was normally finished, the reading unit determines that the read sector is a defective sector, so that the reading unit executes an alternating process. Therefore, even if a defective sector such that the sync byte pattern is lost due to the thermal asperity of the MR head occurs during the use by the user, the defect is eliminated by the alternating process and a growth of the defect during the use by the user can be substantially suppressed.

Detailed Description Text (24):
FIG. 12 shows another embodiment of the write channel 19 in FIG. 1. The embodiment is characterized in that the data, ECC, and gap pattern to be written to the disk medium are scrambled. In a manner similar to the embodiment of FIG. 2, the HDC interface circuit 60 for writing, 8/9 encoder 62, parallel/serial converter 64, precoder 66, frequency divider 68, and driver 70 are provided for the write channel

19. A circuit function to scramble the data, ECC, and gap pattern is provided between the HDC interface circuit 60 for writing and the 8/9 encoder 62. That is, a scrambling circuit 272 is provided subsequently to the HDC interface circuit 60 for writing. The scrambling circuit 272 has an EX-OR circuit 274 and a pseudo random pattern generator 276. The pseudo random pattern generator 276 generates, for example, an (M) series code having a predetermined code length. The EX-OR circuit 274 gets the EX-OR of the formatted data of one sector from the HDC interface circuit 60 for writing and the pseudo random pattern, thereby scrambling. Subsequent to the scrambling circuit 272, a selecting circuit 270 is provided. The data from the HDC interface circuit 60 for writing and the data scrambled by the scrambling circuit 272 are inputted to the selecting circuit 270. Either one of the data is selected and inputted to the 8/9 encoder 62. The selecting circuit 270 selects the data which was scrambled by the scrambling circuit 272 at the timings of the write data, ECC, and gap pattern and selects the data from the HDC interface circuit 60 for writing, namely, the data that is not scrambled in the other timings. The selection of the selecting circuit 270 and the pattern generation of the pseudo random pattern generator 276 are controlled by a timing generating circuit 284. A sync byte detecting circuit 278 and a DL register 280 are provided for the timing generating circuit 284. The sync byte detecting circuit 278 detects and outputs the first and second sync byte patterns SB1 and SB2 included in the formatted write data derived from the HDC interface circuit 60 for writing. The total data length DL of the data DATA and the ECC subsequent to the first sync byte pattern SB1 has been set in the DL register 280. An interval of the data DATA corresponding to the data length DL set in the DL register 280 is set from the timing when the first sync byte pattern SB1 is detected by the sync byte detecting circuit 278. In response to it, the timing generating circuit 284 sets a scrambling period of time for the interval of the data DATA and the ECC. The timing signal indicative of the timing of the data and the ECC which are scrambled due to the timing generating circuit 284 is also supplied to the pseudo random pattern generator 276. The pseudo random pattern is generated from the pseudo random pattern generator 276 to the EX-OR circuit 274 synchronously with the output selection from the scrambling circuit 272 of the selecting circuit 270, thereby enabling the scrambled data to be supplied to the selecting circuit 270.

Detailed Description Text (25):
FIGS. 13A to 13E are time charts for the scrambling process of the write channel 19 in FIG. 12. First, when the write gate signal 81 in FIG. 13A is turned on, the pseudo random pattern generator 276 of the scrambling circuit 272 enters an operable state. In this state, the write data according to the HDC data format as shown in FIG. 13B is inputted to the write channel 19 through the HDC interface circuit 60 for writing. The first sync byte detecting circuit 278 detects the first sync byte pattern 88 shown by SB1 and generates a detection signal to the timing generating circuit 284. In response to it, the timing generating circuit 284 generates a timing signal for the data length DL set in the DL register 280 to the selecting circuit 270, thereby allowing the output of the scrambling circuit 272 to be selected. Since the timing signal is supplied to the pseudo random pattern generator 276, a scrambling signal 288 in FIG. 13D is generated, so that the data DATA 90 and ECC 92 to the EX-OR circuit 274 are scrambled.

Detailed Description Text (26):
FIG. 14 is a block diagram of the embodiment having the descrambling function of the read channel 20 in FIG. 1 corresponding to the write channel 19 having the scrambling function in FIG. 12. The read channel 20 has the amplifier 72, AGC circuit 74, automatic equalizing type maximum likelihood detecting circuit 76, 8/9 decoder 78, serial/parallel converter 79, and HDC interface circuit 80 for reading in FIG. 4. The selecting circuit 124 and memory 126 are provided between the automatic equalizing type maximum likelihood detecting circuit 76 and 8/9 decoder 78 for an error recovery in the case where the sync byte pattern is lost due to the thermal asperity of the MR head. Further, a descrambling circuit 290 and a selecting circuit 304 are provided between the serial/parallel converter 79 and HDC

interface circuit 80 for reading in order to descramble. An EX-OR circuit 292 and a pseudo random pattern generator 294 are provided for the descrambling circuit 290 and this structure is the same as the scrambling circuit 272 in FIG. 12. The selection of the selecting circuit 304 is controlled by a timing generating circuit 305. That is, by selecting an output of the descrambling circuit 290 at the timings of the data DATA and the ECC included in the read data, the descrambling is performed. By directly selecting the output of the serial/parallel converter 79 at the other timings, the descrambling is cancelled. A sync byte detecting circuit 296 is provided to control the serial/parallel converter 79, pseudo random pattern generator 294, and timing generating circuit 305. Further, a DL register 300 in which the total data length DL of the data DATA and the ECC has been stored is provided to control the timing generating circuit 305.

CLAIMS:

4. An apparatus according to claim 1, wherein:

said writing unit has a scrambling circuit for scrambling each of said data and said error detection correction code which are written to said medium by using a predetermined pseudo random code; and

said reading unit has a descrambling circuit for descrambling each of said data and said error detection correction code which were read out from said medium by using said pseudo random code.

10. An apparatus according to claim 7, wherein:

said writing unit has a scrambling circuit for scrambling each of said first and second split data which are written to said medium by using a predetermined pseudo random code; and

said reading unit has a descrambling circuit for descrambling each of said first and second split data which were read out from said medium by using said pseudo random code.

☐ 5. Document ID: US 5930367 A

L12: Entry 5 of 6 File: USPT Jul 27, 1999

DOCUMENT-IDENTIFIER: US 5930367 A
TITLE: Apparatus for recording/reproducing or transmitting/receiving signal data having a portion of an error correction code replaced with other information and methods thereof

Drawing Description Text (7):
FIG. 5 is a diagram of a scrambling circuit for the signal recording apparatus of FIG. 2 according to an embodiment of the present invention;

Drawing Description Text (8):
FIG. 6 is a table of pre-set values for the scrambling circuit of FIG. 5;

Drawing Description Text (9):
FIG. 7 is diagram of a scrambling circuit, in which polynomial and pre-set values may be varied, for the signal recording apparatus of FIG. 2 according to an embodiment of the present invention;

Detailed Description Text (11):
As shown in FIG. 2, the present recording apparatus generally includes an interface circuit 12, a sectoring circuit 13, a scrambling circuit 14, a header appendage circuit 15, an error correction coding (ECC) circuit 16, an identification information substitution circuit 23, a modulation circuit 17, a synchronization appendage circuit 18, and a driving circuit 19.

Detailed Description Text (12):
Digital data, such as digital audio signals, digital video signals, computer data or the like, may be supplied to an input terminal 11. The input digital data is supplied by way of the interfacing circuit 12 to the sectoring circuit 13, whereupon the data is arranged or sectorized in terms of a predetermined data amount (such as 2048 bytes as shown in FIG. 1) so as to form units. The sectorized data is supplied to the scrambling circuit 14 so as to be scrambled or randomized such that the same byte pattern does not appear in succession so as to enable signals to be read and written appropriately. The scrambled or randomized data is supplied to the header appendage circuit 15, wherein header data (such as sector addresses) are arranged at a leading end of each sector, and error detection and correction codes EDC are arranged in a manner as previously described. Output data of the header appendage circuit 15 is supplied to the error correction encoding circuit 16 which may delay the received data and perform parity calculations so as to form parities C1 and C2 which are added to the data.

Detailed Description Text (18):
As an alternative to the above-described arrangement of the recording apparatus of FIG. 2, the scrambling circuit 14 may be provided downstream of the header appendage circuit 15 whereupon the header digital data is scrambled by the scrambling circuit 14 and the resulting scrambled data is supplied to the error correction encoding circuit 16. Additionally, and as hereinafter more fully described, the scrambling circuit 14 may also be utilized to cipher the output data of the sectorizing circuit 13 by varying the scrambling parameters based on the identification information from the interfacing circuit 12.

Detailed Description Text (24):
The error correction decoding circuit 116 performs a decoding or processing operation which is substantially a reverse operation of that performed by the error correction encoding circuit 16 (FIG. 2). The processing performed by the error correction decoding circuit 116 may correct errors caused by defects or flaws in the recording medium 21 or errors obtained during the reproduction of recorded data. Furthermore, the error correction decoding circuit 116 may remove the identification information included in the data received from the demodulation circuit 115 so that the data supplied from the error correction decoding circuit does not include such identification information. The output data of the error correction decoding circuit 116 may be formed or resolved into sectors by the sector resolution circuit 117. An output of the sector resolution circuit 117 is supplied to the header separation circuit 118 wherein the header information may be separated from the received data and the leading portion of each sector is freed. The sector resolution circuit 117 and the header separation circuit 118 are respective counterpart circuits of the sectorizing circuit 13 and the header appendage circuit 15 (FIG. 2). An output of the header separation circuit 118 is supplied to the descrambling circuit 119 wherein a descrambling operation is performed which is substantially opposite to the scrambling operation performed by the scrambling circuit 14 (FIG. 2). Descrambled output data from the descrambling circuit is supplied by way of the interfacing circuit 120 to an output terminal 121.

Detailed Description Text (25):
If the signal recorded on the medium 21 had been ciphered in accordance with the identification information by, for example, the scrambling circuit 14, the reproduced signal is deciphered accordingly. That is, the identification information extracted by the identification information extraction circuit 130 is also supplied to a deciphering circuit, which may be included in the descrambling circuit 119, wherein the signal is deciphered by utilizing the identification information. As is to be appreciated, if the recorded signal had been ciphered using the identification information and the proper identification information is unavailable or not provided during signal reproduction such that the correct identification information is not supplied to the deciphering circuit, then the data may not be deciphered or decoded properly.

Detailed Description Text (31):
Processing performed by the scrambling circuit 14 and a procedure for ciphering the data signals produced therein based on the identification information will now be described.

Detailed Description Text (32):
The scrambling circuit 14 may include a so-called parallel block synchronization type scrambler having a 15-bit shift register 41 as, for example, illustrated in FIG. 5. The scrambling circuit 14 may further include an address detector 75, a register 76, and ExOR circuits 42 and 43. An output from the sectoring circuit 13, which may include sector address information, is supplied to the address detector 75. A detected signal or address from the address detector 75 is supplied to the register 76, whereupon an output signal which may represent pre-set values is supplied to the register 41. Such pre-set or initial values, which may have values such as those shown in FIG. 6, may be set in the 15-bit shift register 41. (The pre-set values in FIG. 6 are expressed in hexadecimal form.) The selection numbers associated with the pre-set values shown in FIG. 6 correspond to the lower four bits of the sector addresses so that the pre-set values may be switched on a sector basis. The 15-bit shift register 41 may include a feedback loop form in accordance with a generating polynomial x.sup.15 +x.sup.n +1 which uses the ExOR circuit 42. A bit clock signal may be supplied through an input bit clock terminal to the register 41. Such bit clock may be utilize to control the bit shifting performed by the register 41. Output data from the shift register 41 is supplied to the ExOR circuit 43 which also receives data from the sectorizing circuit 13 through a data input terminal 35. Such input data may be supplied in a so-called LSB first sequence in which the LSB side is temporally provided first. The input data is processed or ExORed by the ExOR circuit 43 and an output signal therefrom is supplied through an output terminal 44 to the header appendage circuit 15 (FIG. 2).

Detailed Description Text (33):
The above-mentioned polynomial and pre-set (initial) values may be varied in accordance with the identification information by using a scrambling circuit such as that illustrated in FIG. 7. As shown therein, such scrambling circuit 14' may include a register 76', an identification detector 78, a changeover switch 46, a shift register 41, and ExOR circuits 42 and 43. Identification information from the interface circuit 12 (FIG. 2) may be supplied through an input terminal 47 to the identification information detector 78 whereupon a control signal based on the detected identification information, which may be the lower four bits thereof, is supplied to the register 76'. Pre-set values may be stored in the register 76' and, in accordance with the control signal from the identification information detector 78, selected one(s) of the stored pre-set values may be supplied to the register 41, which may be a 15 bit shift register. A bit clock signal for controlling bit shifting may be supplied through an input bit clock terminal to the register 41. Outputs of the respective bits of the 15-bit shift register 41 may be supplied to fixed contacts of the changeover switch 46 which may be controlled by an output

signal (such as the 4-bit control data signal) from the identification information detector 78. Output data from the changeover switch 46 and an output from the register 41 may be supplied to the ExOR circuit 42 so as to form a feedback loop similar to that previously described with reference to the scrambling circuit 14 of FIG. 5. Output data from the shift register 41 and data from the sectorizing circuit 13 through a data input terminal 35 are supplied to the ExOR circuit 43, whereupon the data may be processed or ExORed by the ExOR circuit 43 and supplied through an output terminal 44 to the header appendage circuit 15 (FIG. 2) in a manner similar to that previously described with reference to the scrambling circuit 14 of FIG. 5.

Detailed Description Text (36):
The arrangement of varying the polynomial is not limited to that described above with reference to FIG. 7. For example, a scrambling circuit having a different number of stages or taps in the shift register may be utilized. Additionally, control signals representing other than the lower four bits may be used.

Detailed Description Text (40):
With regard to the reference identification information recorded on the record medium, as described in the explanation of the recording apparatus in FIG. 2, the reference identification information may be recorded in the TOC of the record medium 21, the reference identification may be read out by the recording/reproducing head 20. Also, the reference identification information may be stored at a site on the recording medium 21 which may be specified on a sector basis by storage site information, or alternatively, may be stored on sites other than those on the recording medium 21. The storage site information may be recorded in a table of contents (TOC) area or in another predetermined sites. As an example, the storage site information may be stored as part of the TOC information in the lead-in area 103 of the record medium 21. This arrangement may protect against alteration of the reference identification information. During reproduction, the storage site information is read out and, based thereon, the reference identification information for deciphering may be obtained. In addition to being recorded on the record medium 21, the reference identification information may be recorded on the medium by other recording techniques, such as those involving bar codes, wobbling or UV rays. Furthermore, as previously described, the reference identification information may be stored on sites other than those on the recording medium 21. Such other sites may be an EEPROM or in an information storage device connected to or included within the reproducing apparatus, such as IC card or a so-called PCMCIA (personal computer memory card international association). Additionally, the reference identification information may be supplied from a communication apparatus such as a modem/LAN via a communication interface or from an external device through the communication interface or from a remote controlled device by way of a remote-controlled reception device.

☐ 6. Document ID: US 4084196 A

L12: Entry 6 of 6 File: USPT Apr 11, 1978

DOCUMENT-IDENTIFIER: US 4084196 A
TITLE: Electronic half-tone generating means for facsimile reproduction system

Detailed Description Text (44):
The vertial and horizontal flag signals developed by detector 323 are input through

multiplexer 320 to flag store RAMs 366 and 368 contained in storage units 347 and 348 and are read out therefrom onto a line 367 for input to delay line 353. RAMs 366 and 368 are each one line storage devices into which the flag signals of the corresponding three scan lines are ORed. The output of delay line 353 is used to select either the delayed scrambled mezzo data at terminal 355 or the screen cell data at terminal 357 for input to transmitter 304.

Detailed Description Text (46):
In FIG. 19 the operative components of logic 349, formatter 350, and converter 351 are schematically illustrated. As indicated, logic 349 includes cell address and switching circuitry which functions to address those bits of data in store 347 or data in store 348 which correspond to a particular data cell to be processed. Circuitry 370 also selects the corresponding flag signal for output on line 367. Formatter 350, which is in essence a data scrambling circuit, includes three five-bit series-to-parallel shift registers 380, 382, and 384, the parallel outputs of which are fed into a multiplexer 386.

Terms	Documents
L1 and L10	6

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☐ 1. Document ID: US 6668349 B1

L12: Entry 1 of 6 File: USPT Dec 23, 2003

DOCUMENT-IDENTIFIER: US 6668349 B1
TITLE: Data recording/readback method and data recording/readback device for the same

Brief Summary Text (5):
Also, conventional technologies generally use error correction coding technologies. The reliability of decoded data is improved by performing detection and correction of errors during readback for decoding errors generated after decoding data using the maximum-likelihood technique described above. An example of this error correction coding (ECC) technology is the combination error correction coding technology that uses the interleaving technique and Reed-Solomon coding. This is used in many information storage devices, including magnetic disk devices and optical disk devices. Thus, it is possible to detect and correct errors in the decoded data generated from the various factors described above including random decoding errors caused during data decoding by noise. This allows a high degree of reliability to be maintained in the decoding and readback of data stored in high-density storage/readback devices. Implementations of this type of error correction coding technology can be found, for example, in R. D. Cydecyan, "A PRML system for Digital Magnetic Recording" (IEEE Journal on Selected Areas in Communications, Vol.10, No.1, 1992) as well as in Japanese Laid-open Patent Publication number 11-168514 (U.S. application Ser. No. 09/124,840). For increasing storage density in information recording/readback devices and improving reliability in data decoding and readback, the main technologies are PRML signal processing, which provides a data decoding technique based on the maximum likelihood sequence estimation referred to above, and error detection/correction coding.

Drawing Description Text (11):
FIG. 6 is a schematic diagram showing a sample operation performed by a scrambling circuit from a second embodiment of the present invention.

Detailed Description Text (46):
FIG. 5 shows a second embodiment of the present invention. This embodiment differs from the embodiment shown in FIG. 1 in that a code scrambling circuit 30a for changing the code sequence of the record information code sequence 1b is interposed between the error data detection/correction encoder 2 and the recording/readback-system channel 3. Also, a reverse code scrambling circuit 30b corresponding to the code scrambling circuit 30a and changing the code sequence of an code sequence input in the opposite direction is interposed between the maximum-likelihood sequence decoder 7 and the error data detector/corrector circuit 8. The code sequence changed by the code scrambling circuit 30a is restored to the original code sequence by the reverse code scrambling circuit 30b. The code position information 8f and the code information 8g takes the ordering of the code sequence

at the input and output of the reverse code scrambling circuit 30b into account and performs appropriate conversions via a similar code scrambling circuit 30a so that there are no inconsistencies between the code position information and the corresponding code information. The purpose behind the code scrambling circuits 30a and the reverse code scrambling circuit 30b is to disperse the error codes from decoding error propagation generated in the maximum-likelihood sequence decoder 7 in the plurality of interleaved error code sequences. This allows sections of error codes in decode error propagation to be more easily corrected by the error data detector/corrector 8. By increasing the probability that a section of error code within decoding error propagation can be corrected in the decoder 8c of the error data detector/corrector 8, the probability is increased that when the corrected code information is fed back, the decoding operation performed by the maximum-likelihood sequence decoder 7 will be able to eliminate the decoding error propagation.

Detailed Description Text (47):
FIG. 6 shows an example of the change in code sequence performed by the code scrambling circuit 30a used in this embodiment as shown in FIG. 5. In this embodiment, the record information code sequence 1a is interleaved as four code sequences 21a-21d using code blocks 20 (shown in the figure as squares with thick lines) as units. Reed-Solomon error correction coding is performed on each of the codes, and error checking code blocks 22a-22d are added to each of the code sequences. The Reed-Solomon error correction coding is performed on each code block 20. In this embodiment, the code blocks 20 are divided into record code blocks 31 having half the code length. The code scrambling circuit 30a uses these blocks as the processing unit and changes the code sequence as indicated by the sequence of numbers added to the blocks in the figure. As the figure shows, the code length of the record code blocks 31 are set to be smaller than the code lengths of the code blocks 20. The code scrambling circuit 30b changes the code sequence so that the record code blocks 31 recorded consecutively on the recording medium are, separated by at least a predetermined code length after being output from the code scrambling circuit 30b. As a result, the recording code blocks 31 that are recorded consecutively on the recording medium are positioned at different code sequences 31a-21d in the error data checker/corrector 8. The code blocks 31 have a shorter code length than the code blocks 20 so that decode errors from maximum-likelihood sequence decoding that occur in a single code block 20 tend to be separated into different code sequences 21a-21d. As a result, sections of decoding propagation that have code lengths of at least half that of the code block 20 (i.e., the code length of the record code block 31) will be more easily corrected in one of the independent code sequences 21a-21d. By repeatedly feeding back the error correction information and the performing maximum-likelihood sequence decoding, the probability that the decoding errors will all be eliminated is increased. By providing code scrambling circuits in the maximum-likelihood sequence decoder 7 and the error detector/corrector 8, the effectiveness of correcting decoding errors is increased in the present invention.

☐ 2. Document ID: US 6587975 B2

L12: Entry 2 of 6 File: USPT Jul 1, 2003

DOCUMENT-IDENTIFIER: US 6587975 B2
TITLE: Semiconductor test apparatus and method